

ABSTRACT OF THE DISCLOSURE

A signal processor provides stable processing, for each frame, of variable-length coded data. An MPEG stream is input in the SDTI format, and a data active length for each frame is determined based on header information for each SDTI frame to generate a "Frame End" signal which is synchronized with the end-of-frame data. The "Frame End" signal is input to a set terminal of an RS flip-flop circuit via a delay circuit. On the other hand, a start code at the beginning of a frame is detected by a detector circuit and an OR circuit, and the result of detection is input to a reset terminal of the RS flip-flop circuit. A switching control is performed so that an enable signal indicates invalid data when the frame end pulse is detected and the enable signal indicates valid data when the start code is detected in response to the output of the RS flip-flop circuit. The data is invalid in a period from the end of a frame until the next start code has been detected, and thereby reducing the processing delay while providing a stable operation for irregular stream inputs.